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APPLICATION FOR LETTERS PATENT

FOR

ETCH OF SILICON NITRIDE SELECTIVE TO SILICON AND SILICON DIOXIDE USEFUL DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

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ETCH OF SILICON NITRIDE SELECTIVE TO SILICON AND SILICON DIOXIDE USEFUL DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

Field of the Invention

[0001] This invention relates to the field of semiconductor manufacture and, more particularly, to an etch useful for removing silicon nitride selective to silicon and silicon dioxide.

Background of the Invention

[0002] During the manufacture of semiconductor devices such as a memory devices, logic devices, and microprocessors, various processes are commonly performed. Etching silicon nitride selective to silicon (such as polysilicon) and to silicon dioxide with various etch ratios is often required. For example, hot phosphoric acid isotropically etches silicon nitride selective to silicon dioxide and silicon. Other processes for etching Si_3N_4 selective to SiO_2 and Si are discussed in *"Highly Selective Etching of Silicon Nitride Over Silicon and Silicon Dioxide,"* J. Vac. Sci. Technol. A 17(6), Nov/Dec 1999, which describes the use of oxygen (O_2) and nitrogen (N_2) in combination with CF_4 or NF_3. The processes discussed achieve Si_3N_4 to Si and to SiO_2 etch rate ratios of up to 100 and 70 respectively using nitrogen trifluoride. The processes uses high flow rates of 800 standard cubic centimeters (sccm) O_2 and 110 sccm N_2 for most experiments. Further, using carbon tetrafluoride, a Si_3N_4 to polysilicon etch ratio of 40 was achieved while SiO_2 was not etched at all. Etch rates of silicon nitride are below about 50 angstroms (Å) per minute.

[0003] As semiconductor manufacture typically requires high volume processing to lower costs, any decrease in temporal processing requirements can result in a large increase in product throughput. Further, having options available to accomplish a task such as etching silicon nitride is advantageous, as one process may function better for certain manufacturing flows. Additional methods for etching silicon nitride selective to silicon and silicon nitride at an accelerated rate would be desirable.

Summary of the Invention

[0004] The present invention provides a new etch method that, among other advantages, reduces problems associated with the manufacture of semiconductor devices, particularly problems in etching silicon nitride selective to silicon and silicon dioxide. In accordance with one embodiment of the invention a semiconductor wafer substrate assembly having a layer of silicon nitride and a layer of at least one of silicon and silicon dioxide is placed into an etch chamber. Oxygen and either CHF_3 or CH_2F_2 are introduced into an etch chamber under controlled flow rates, power, and pressure. At the parameters detailed herein, the etch removes silicon nitride selective to silicon dioxide and silicon.

[0005] Additional advantages will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

Brief Description of the Drawings

[0006] FIG. 1 depicts a cross section of a semiconductor wafer assembly including a blanket layer of silicon nitride; and

[0007] FIG. 2 depicts the cross section of FIG. 1 subsequent to an etch to form silicon nitride spacers.

[0008] It should be emphasized that the drawings herein may not be to exact scale and are schematic representations. The drawings are not intended to portray the specific parameters, materials, particular uses, or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

Detailed Description of the Preferred Embodiment

[0009] A silicon nitride etch selective to silicon (such as monocrystalline or polycrystalline silicon) and to silicon dioxide comprises the use of O_2 and either CHF_3 or CH_2F_2 at relatively low flow rates. It should be noted that the parameters described herein are optimized for an Applied Materials 5000 (AME5000) etcher, but they may be converted easily by one of ordinary skill in the art for other systems.

[0010] In accordance with one embodiment of the invention, a semiconductor wafer having a layer of silicon nitride and a layer of silicon dioxide and/or silicon is placed into an etch chamber and subjected to an etch. This embodiment of the etch comprises an O_2:CHF_3 or O_2:CH_2F_2 flow rate ratio of greater than about 3:1, which results in a relatively rapid, controllable Si_3N_4 etch rate with good selectivity to Si and to SiO_2. For example, an O_2 flow rate of between about 20 sccm and about 80 sccm and a CHF_3 or CH_2F_2 flow of between about 5 sccm and about 25 sccm would be sufficient. More preferably, an O_2 flow rate of between about 35 sccm and about 60 sccm and a CHF_3 or CH_2F_2 flow of between about 10 sccm and about 20 sccm would be sufficient, and most preferably an O_2 flow rate of about 60 sccm and a CHF_3 or CH_2F_2 flow of about 20 sccm would be sufficient.

[0011] During the etch, a pressure of between about 10 millitorr to about 60 millitorr is maintained. More preferably, a pressure of between about 30 to about 60 millitorr, and most preferably, between about 30 to about 40 millitorr is maintained. Further, a power of between about 300 watts to about 600 watts, more preferably between about 300 watts to about 500 watts, and most preferably between about 300 to about 400 watts sustained within the chamber. With increasing power and/or pressure the etch rate increases and the selectivity to Si and SiO_2 decreases.

[0012] Using the parameters described above, it is estimated that an Si_3N_4:SiO_2 etch ratio of up to about 1.3:1 on a blanket film and up to about 3:1 over topography can be achieved, as well as an Si_3N_4:Si etch ratio of up to about 7:1. As the O_2:CHF_3 or O_2:CH_2F_2 increases beyond 3:1 the etch rate of the Si_3N_4 decreases and the selectivity to

Si and SiO_2 increases. With a high O_2:CHF_3 or O_2:CH_2F_2 ratio, above about 10:1, the etch rate becomes so slow as to be decreasing usefulness in most instances. As the O_2:CHF_3 or O_2:CH_2F_2 ratio decreases further below 3:1 the etch removes Si_3N_4 at an increased rate but also becomes less selective to Si and SiO_2. An O_2:CHF_3 or O_2:CH_2F_2 ratio of about 3:1 is believed to provide a good balance between nitride etch rate and selectivity to Si and SiO_2 in many uses of the invention for semiconductor manufacture.

[0013] At a pressure of about 30 millitorr, a power of 300 watts, a CHF_3 or CH_2F_2 flow rate of 20 sccm, and an O_2 flow rate of 60, the etch rate of Si_3N_4 will be about 420 Å/min. With a pressure of 40 millitorr, a pressure of about 40 millitorr, a power of 300 watts, a CHF_3 or CH_2F_2 flow rate of about 10 sccm and an O_2 flow rate of about 40 sccm, the etch rate increases to about 904 Å/min. As the CHF_3/O_2 or CH_2F_2/O_2 ratio increases the Si_3N_4 etch rate increases, such that at a pressure of 30 millitorr and a power of 300 watts, and a flow rate of 35 sccm for both O_2 and CHF_3 or CH_2F_2 the etch rate increases to about 1270 Å/min. These processes use a chuck temperature of about 10°C and a sidewall temperature of about 20°C.

[0014] Using the preferred parameters of the instant invention as discussed above results in an anisotropic nitride etch which removes nitride from horizontal surfaces faster than it removes nitride from vertical surfaces at an etch ratio of about 3.7:1. This is especially useful for etching structures similar to those depicted in FIGS. 1 and 2, as it allows sufficient etching to remove the nitride layer from the wafer surface without damaging the silicon wafer. The structure of FIG. 1 depicts a semiconductor substrate assembly 10 comprising a semiconductor wafer 12, field oxide 14, doped transistor source/drain regions 16 within the wafer 12, and a transistor gate stack comprising gate oxide 18, polycrystalline silicon (polysilicon) 20, a conductive silicide layer 22, and an oxide or nitride layer 24, for example tetraethyl orthosilicate (TEOS) or silicon nitride. FIG. 1 further depicts a blanket silicon nitride layer between about 300Å about 600Å thick. Such a structure can be manufactured by one of ordinary skill in the art.

[0015] The structure of FIG. 1 is subjected to an inventive etch as described above. An exemplary etch includes processing the wafer in a chamber of an AME5000 etch chamber. After placing the wafer substrate assembly in the etch chamber, O_2 and CHF_3 or CH_2F_2 are introduced into the chamber at flow rates of about 60 sccm and about 20 sccm respectively. Pressure is maintained at between about 30 millitorr and about 40 millitorr, and a power of between about 300 watts and about 400 watts is utilized. At a chuck temperature of about 10°C and a sidewall temperature of about 20°C, the silicon nitride will etch at a rate of about 720Å/min in the vertical direction, and about 180Å/min in the horizontal direction. Generally, the vertical:horizontal etch rate will be about 4:1. For the 525Å thick layer of silicon nitride depicted in FIG. 1, the etch is performed for between about 35 seconds and about 60 seconds which results in the structure of FIG. 2. Spacers 32 having a width of about 300Å to about 400Å are formed.

[0016] The etch detailed above provides a silicon nitride etch which is selective to silicon and silicon dioxide. This is accomplished using the etch as described consisting essentially of a flow of O_2 and CHF_3 or CH_2F_2. The addition of hydrogen from CHF_3 or from CH_2F_2, in addition to providing an etch of silicon nitride selective to silicon and silicon dioxide, further provides an etch which results in a more square profile of the completed transistor structures than conventional etches. The relatively low flow rates of CHF_3 or CH_2F_2 may also contribute to the less rounded feature profile compared with conventional etches having high gas flow rates. Rounded profiles may adversely affect the self-aligned contact (SAC) etch performance, and possibly affect the electrical properties of the device. In extreme cases, conventional etches can expose the conductive polysilicon, metal, or silicide which is protected by the oxide. Additionally, the structure depicted in FIG. 1, and other similar structures, can be etched with less concern for damaging the silicon wafer once the nitride has been cleared due to the high selectivity to silicon.

[0017] A semiconductor device formed in accordance with the invention may be attached along with other devices to a printed circuit board, for example to a computer motherboard or as a part of a memory module used in a personal computer, a minicomputer, or a mainframe. A device formed in accordance with the invention could further be useful in other electronic devices related to telecommunications, the automobile industry, semiconductor test and manufacturing equipment, consumer electronics, and virtually any consumer or industrial electronic equipment.

[0018] While this invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.